

```
graph TD
    112[CONTENT SOURCE DESTINATION STORAGE 112]
    114[SYSTEM RENEWAL SUBSYSTEM 114]
    116[AUTHENTICATION AND KEY EXCHANGE SUBSYSTEM 116]
    118[IEEE 1394 INTERFACE 118]
    120[CONTENT CIPHER SUBSYSTEM 120]
    100[C.E. DEVICE 100]
    122[IEEE 1394 INTERFACE 122]

    112 --> 116
    112 --> 120
    116 <--> 114
    116 --> 120
    120 <--> 118
    118 --> 122
```

PRIOR ART

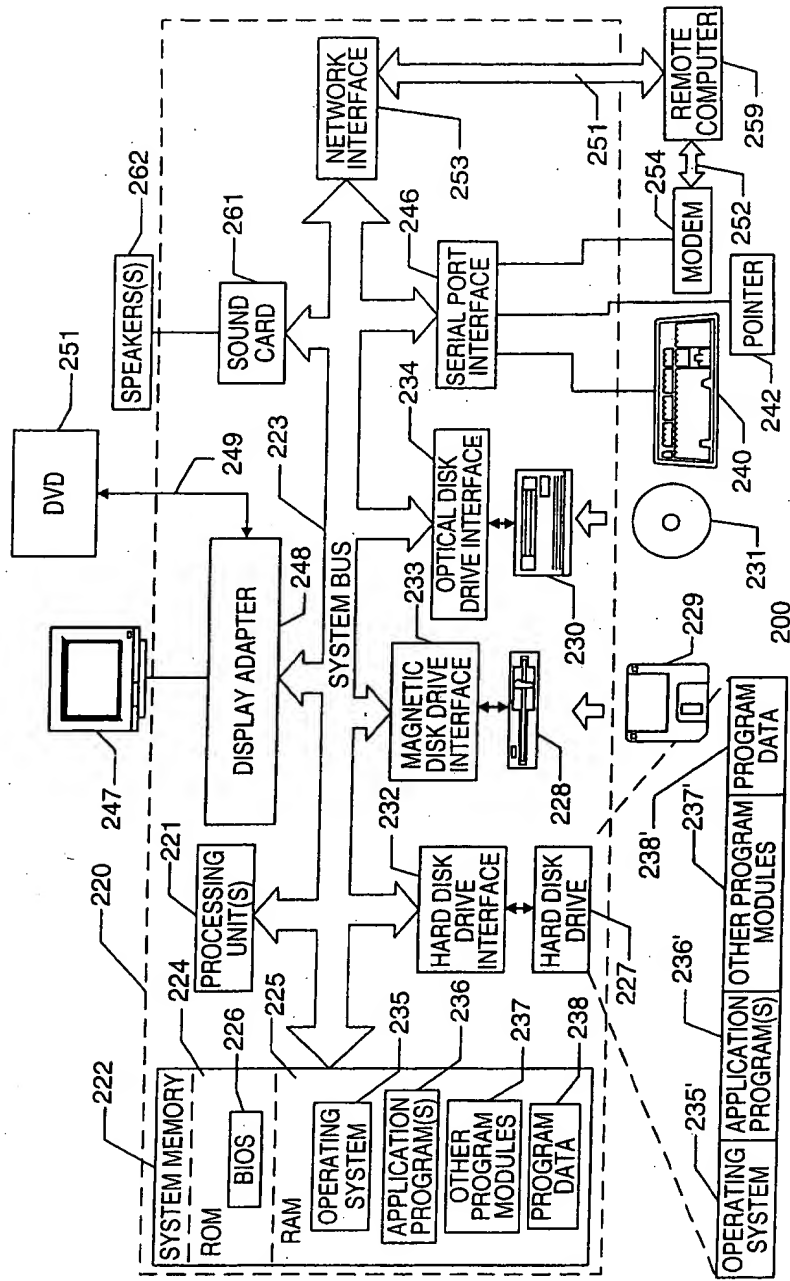


FIG. 2

THE

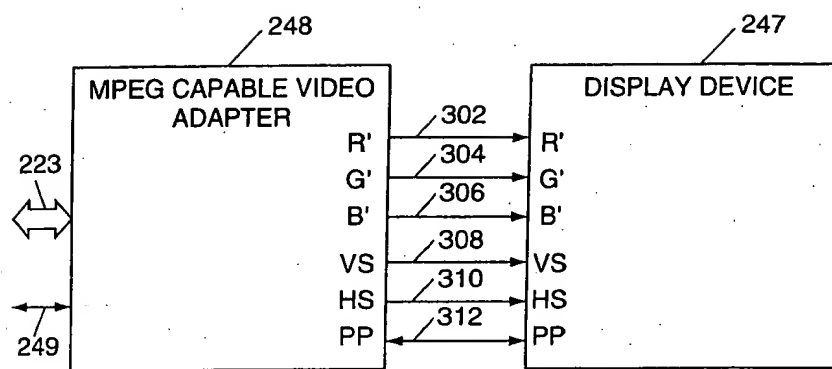


FIG. 3

```

graph TD
    350(( )) --> 352([START - INITIATE DISPLAY ADAPTER  
OPERATION AND REQUEST IDENTIFICATION  
INFORMATION FROM ANY DISPLAY DEVICE  
COUPLED TO THE DISPLAY ADAPTER])
    352 --> 354[MONITOR FOR RESPONSE FROM  
DISPLAY DEVICE]
    354 --> 356{HAS A  
RESPONSE BEEN DETECTED  
WITHIN PRESELECTED TIME  
PERIOD?}
    356 -- Y --> 358[EXAMINE  
IDENTIFICATION  
INFORMATION]
    356 -- N --> 362[RESTRICT VIDEO  
ADAPTER OUTPUT TO  
VIDEO INFORMATION  
NOT SUBJECT TO  
ENCRYPTION  
RESTRICTION]
    358 --> 360{IS THE  
DISPLAY A LINE  
SWAPPING CAPABLE  
DISPLAY?}
    360 -- Y --> 366[EXCHANGE SESSION  
KEY AND  
SYNCHRONIZATION  
INFORMATION WITH  
DISPLAY DEVICE ON  
PERIODIC BASIS]
    360 -- N --> 364[OUTPUT R, G, B VIDEO  
SIGNALS IN FIRST,  
SECOND AND THIRD  
LINES RESPECTIVELY]
    366 --> 368[OUTPUT VIDEO  
SIGNALS ON FIRST,  
SECOND AND THIRD  
LINES AS A FUNCTION  
OF PSEUDO RANDOM  
NUMBER GENERATOR  
OUTPUT]
    362 --> 364
    364 --> 368
    368 --> 370([STOP])

```

FIG. 4

FIG. 5

000000" 5T050050

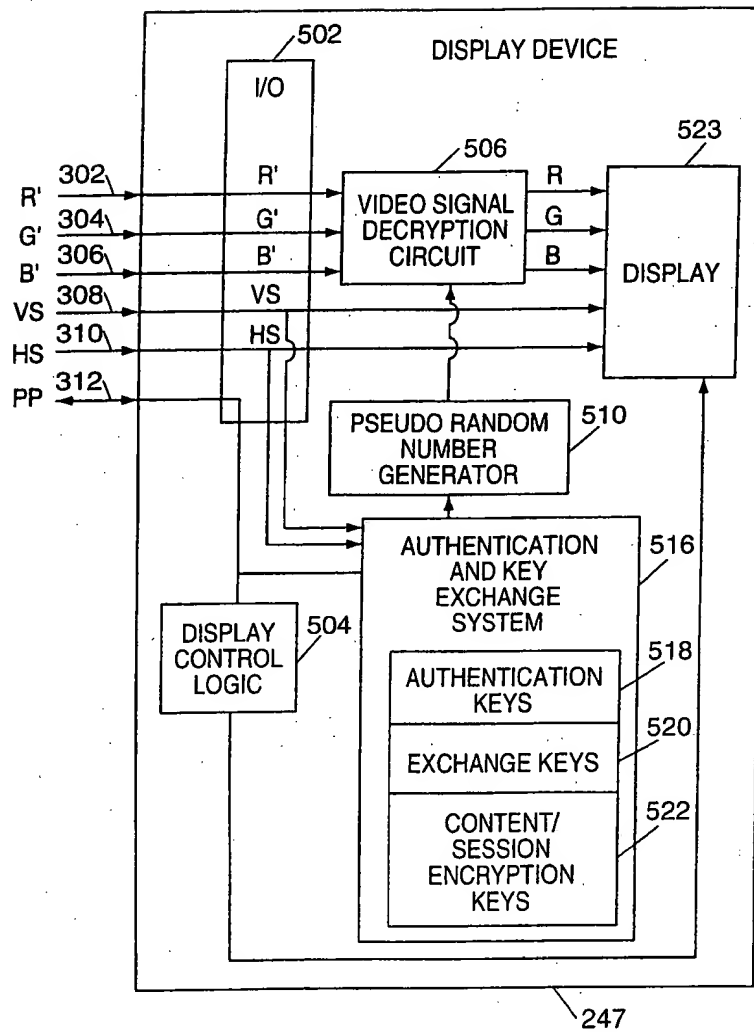


FIG. 6

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad 602$$

FIG. 7

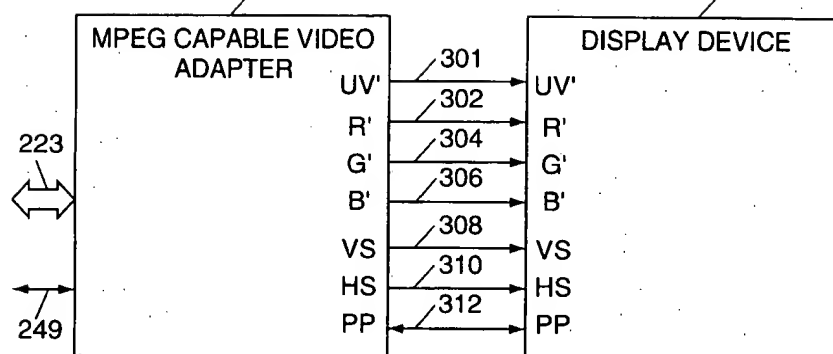


FIG. 8

The diagram illustrates a video display system (848) with the following components and connections:

- DISPLAY ADAPTER (848)**: The central processing unit containing:
 - VIDEO PROCESSOR**: Receives video signals (R, G, B) and control signals (CTRL, VS, HS, PP) from the I/O block. It outputs UV signals to the UV SIGNAL GENERATOR and encrypted video signals (R', G', B') to the I/O block.
 - VIDEO SIGNAL ENCRYPTION CIRCUIT (906)**: Receives R, G, B signals from the video processor and control signals (VS, HS, PP) from the I/O block. It outputs UV' signals to the UV SIGNAL GENERATOR and encrypted video signals (R', G', B') to the I/O block.
 - I/O (912)**: Manages external connections (902, 302, 304, 306, 308, 310, 312) and internal data flow between the video processor, encryption circuit, and other subsystems.
 - UV SIGNAL GENERATOR (901)**: Generates UV signals based on inputs from the video processor and encryption circuit.
 - CONTROL ROUTINES (407)**: Part of the system's control logic.
 - MEMORY (418)**: Stores authentication keys, exchange keys, and content/session encryption keys.
 - MATRIX INVERTER (908)**: Converts digital video signals into a format suitable for the display.
 - PSEUDO RANDOM NUMBER GENERATOR (910)**: Generates random numbers for cryptographic operations.
- EXTERNAL SUBSYSTEMS**:
 - 1394 CONTENT CIPHER SUBSYSTEM (414)**: Receives content data from the video processor and provides encrypted content to the video processor.
 - AUTHENTICATION AND KEY EXCHANGE SYSTEM (416)**: Manages authentication and key exchange, receiving data from the video processor and providing keys to the encryption circuit and memory.

Signal paths are indicated by arrows, showing the flow of video data, control signals, and cryptographic information throughout the system.

FIG. 9

THE UNIVERSITY OF CHICAGO

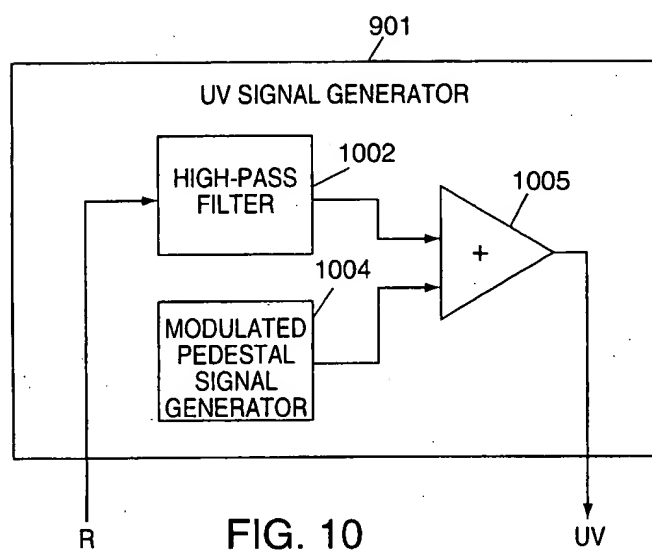


FIG. 10

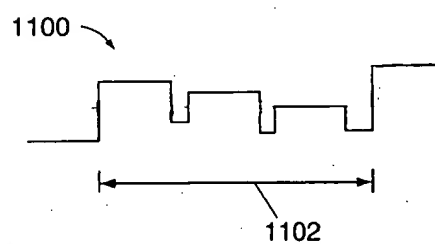


FIG. 11



FIG. 12

Introduction

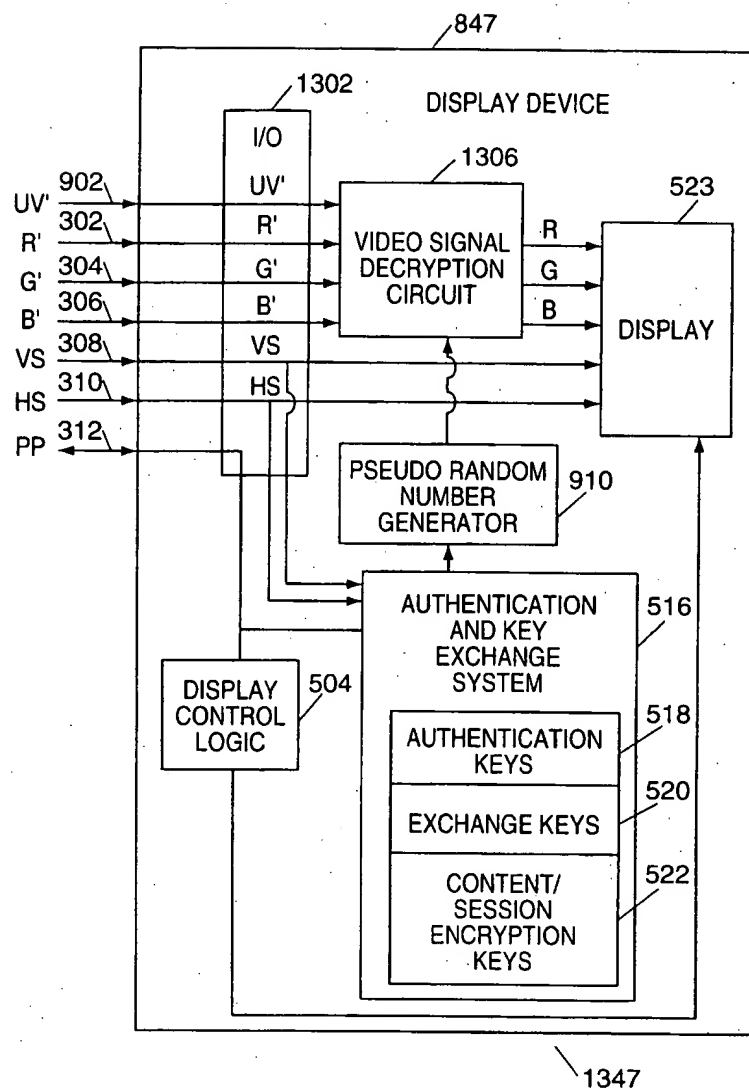


FIG. 13

THE UNIVERSITY OF CHICAGO

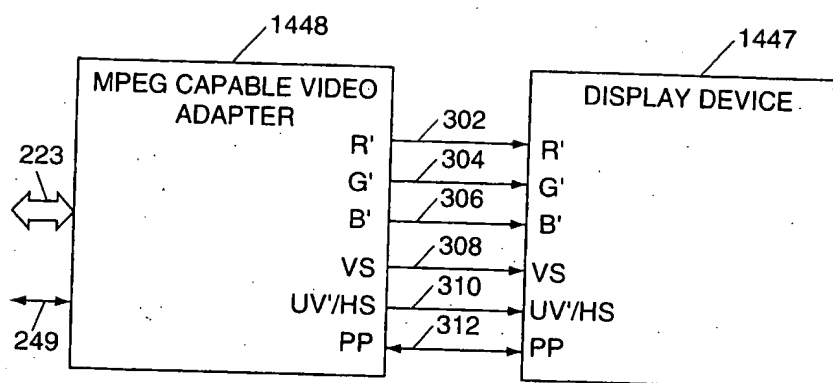


FIG. 14

THE

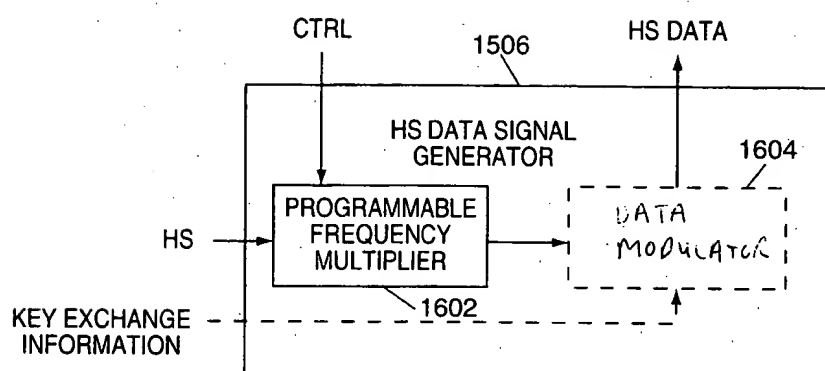


FIG. 16

